In the Claims:

Claims 1-90 (canceled).

Claim 91 (currently amended): An integrated module comprising:

a single interconnect substrate;

a first active circuit chip wire bonded to said single interconnect substrate;

a second active circuit chip interconnected to said single interconnect substrate;

a first ground plane integral to said single interconnect substrate and operatively associated with said first active chip;

a second ground plane integral to said single interconnect substrate and operatively associated with said second active chip;

a first discrete component surface mounted on said single interconnect substrate; and

a second discrete component ~~embedded in~~situated on said single interconnect substrate.

Claim 92 (original): The integrated module of claim 91 wherein said first discrete component is surface mounted using a high-temperature solder.

Claim 93 (original): The integrated module of claim 91 further comprising a solder mask area on said single interconnect substrate.

Claim 94 (original): The integrated module of claim 93 wherein said solder mask area is adjacent to said first discrete component.

Claim 95 (original): The integrated module of claim 91 wherein said first discrete component is selected from the group consisting of an inductor, a transformer, a capacitor, and a resistor.

Claim 96 (original): The integrated module of claim 91 wherein said second discrete component is selected from the group consisting of an inductor, a transformer, a capacitor, and a resistor.

Claim 97 (original): The integrated module of claim 91 wherein said single interconnect substrate comprises a plurality of metal layers and a plurality of dielectric layers.

Claim 98 (original): The integrated module of claim 97 wherein at least one of said plurality of metal layers defines a printed component.

Claim 99 (original): The integrated module of claim 98 wherein said printed component is selected from the group consisting of an inductor, a resistor, a capacitor, and a transformer.

Claim 100 (previously presented): The integrated module of claim 97 wherein at least one of said plurality of metal layers defines one of said first and second ground planes.

Claim 101 (original): The integrated module of claim 91 wherein said first active circuit chip comprises an RF section.

Claim 102 (original): The integrated module of claim 91 wherein said first active circuit chip comprises an IF section.

Claim 103 (previously presented): The integrated module of claim 91 further comprising at least one exposed conductive strip formed on said single interconnect substrate and situated between said first and second active circuit chips, said at least one exposed conductive strip electrically coupled to at least one of said first and second planes.

Claim 104 (original): The integrated module of claim 103 wherein said first and second active circuit chips respectively comprise first and second RF sections.

Claim 105 (original): The integrated module of claim 103 wherein said first active circuit chip comprises an RF section and wherein said second active circuit chip comprises an IF section.

Claim 106 (original): The integrated module of claim 103 wherein said first active circuit chip comprises a CMOS chip and wherein said second active circuit chip comprises a GaAs chip.

Claim 107 (original): The integrated module of claim 97 wherein at least one of said plurality of metal layers defines said first discrete component.

Claim 108 (original): The integrated module of claim 107 wherein said first discrete component is selected from the group consisting of an inductor, a resistor, a capacitor, and a transformer.

Claim 109 (original): The integrated module of claim 97 wherein at least one of said plurality of metal layers defines said second discrete component.

Claim 110 (original): The integrated module of claim 109 wherein said second discrete component is selected from the group consisting of an inductor, a resistor, a capacitor, and a transformer.

Claim 111 (original): An integrated module comprising:

a single interconnect substrate including a plurality of metal layers and a plurality of dielectric layers;

first and second active circuit chips on a top surface of said single interconnect substrate;

a conductive ring formed on said single interconnect substrate, said conductive ring enclosing said first and second active circuit chips;

a conductive strip formed on said single interconnect substrate, said conductive strip situated between said first and second active circuit chips;

a metal lid covering said first and second active circuit chips, said metal lid contacting said conductive ring and said conductive strip, wherein said metal lid, said conductive ring, and said conductive strip substantially prevent electromagnetic interference from reaching said first and second active circuit chips.

Claim 112 (original): The integrated module of claim 111 further comprising a first ground plane below said first active circuit chip, wherein said first ground plane

substantially prevents electromagnetic interference from reaching said first active circuit chip.

Claim 113 (original): The integrated module of claim 112 wherein said first ground plane is defined by at least one of said plurality of metal layers below said first active circuit chip.

Claim 114 (original): The integrated module of claim 112 further comprising a second ground plane below said second active circuit chip, wherein said second ground plane substantially prevents electromagnetic interference from reaching said second active circuit chip.

Claim 115 (original): The integrated module of claim 114 wherein said second ground plane is defined by at least one of said plurality of metal layers below said second active circuit chip.

Claim 116 (original): The integrated module of claim 111 wherein said conductive ring is coupled to ground through a plurality of peripheral vias.

Claim 117 (original): The integrated module of claim 112 wherein said conductive ring is coupled to said first ground plane through a plurality of peripheral vias.

Claim 118 (original): The integrated module of claim 114 wherein said conductive ring is coupled to said second ground plane through a plurality of peripheral vias.

Claim 119 (original): The integrated module of claim 111 wherein said conductive strip is coupled to ground through a plurality of peripheral vias.